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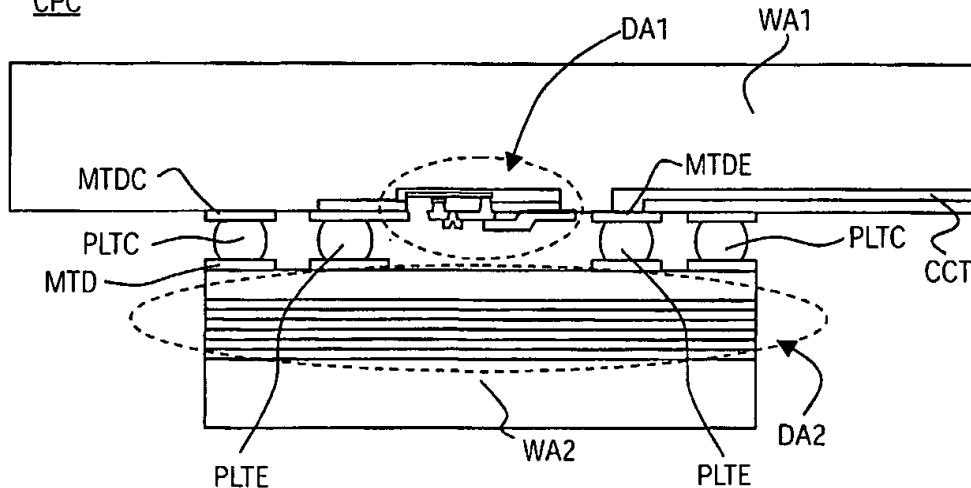
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(54) Title: CHIP STACK WITH INTERMEDIATE CAVITY

CPC



(57) Abstract: The invention relates to a method for connecting a connecting surface of a first silicon wafer [WA1] with a connecting surface of a second silicon wafer [WA2] so as to form an insulated cavity after assembly, at least one of the two silicon wafers [WA] including at least one functional area [DA] intended to be within the cavity. The method according to the invention includes a step [PLTS] of depositing alloy soldering bumps [PLTC] on the connecting surface of the first silicon wafer [WA1], said bumps [PLTC] being separated from one another by an even distance which is sufficiently small to cause joinings during the assembly of the two silicon wafers. Said step [PLTS] of depositing the soldering bumps [PLTC] is carried out during the step of depositing the soldering bumps [PLTE] intended for the electrical contacts. The method includes a reflux soldering step [RFX] for assembling the two silicon wafers by melting of the alloy soldering bumps. Application: Protection of semiconductor elements sensitive to the external conditions.

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## INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L25/065 H01L23/00 H01L21/50 H01L23/10 H01L21/60

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 951 068 A (IMEC INTER UNI MICRO ELECTR ;C P CLARE CORP (US)) 20 October 1999 (1999-10-20) Y claims 1,8,13-15; figures 5,6 ---	1,3-6
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Y	US 6 097 097 A (HIROSE TATSUYA) 1 August 2000 (2000-08-01) A figure 1C ---	2
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 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

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